b. Amendments to the Specification

Please Amend the Title as follows:

APPARATUS WITH IMPROVED LAYERS OF GROUP III-NITRIDE SEMICONDUCTOR

Delete the 2 paragraphs at page 2 between lines 7 and 26.

Rewrite the paragraph between page 2, line 27, and page 3, line 2, as follows:

In ~~a~~ one ~~second~~ aspect, the invention features apparatus with ~~method for electrically passivating threading defects in~~ layers of group III-nitride semiconductors having electrically passivated threading defects. The electrical passivation lowers the conductivity of a defect so that a passivated defect does not carry a higher current density than the surrounding semiconductor matrix. Thus, electrical passivation reduces the effect of threading defects on the conductivity through the layer of group III-nitride semiconductor and thereby reduces defect-induced shorting in such layers.

Rewrite the paragraph at page 3, lines 3 – 7 as follows

In this ~~the second~~ aspect, various embodiments provide ~~a method for fabricating vertical electronic devices. The method includes epitaxially growing a layer of group III-nitride semiconductor on a crystalline substrate and then, chemically treating an uncovered surface of the layer to selectively electrically passivate defects that thread the layer of semiconductor~~ an apparatus that includes a crystalline substrate having a top surface, a crystalline semiconductor layer located on the top surface, and a plurality of dielectric regions. The crystalline semiconductor layer includes group III-nitride and has first and second surfaces. The first surface is in contact with the top surface of the substrate. The second surface is separated from the top surface by semiconductor of the crystalline semiconductor layer. The dielectric regions are located on the second surface. Each dielectric region is distant from the other dielectric regions and covers an end of an associated lattice defect. Each lattice defect threads the crystalline semiconductor layer.